Current Mode Class-D Power Amplifiers for High Efficiency RF Applications

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***Abstract* — We show that current mode class-D (CMCD) power amplifiers can achieve high efficiency at RF frequencies. In contrast with conventional voltage-mode Class D amplifiers, the CMCD features "zero voltage switching" which eliminates the output capacitance discharge loss. Experimental CMCD amplifiers with 76.3% PAE at 290mW output and 71.3% PAE at 870mW output are demonstrated, using GaAs FETs at 900MHz.**

I. Introduction

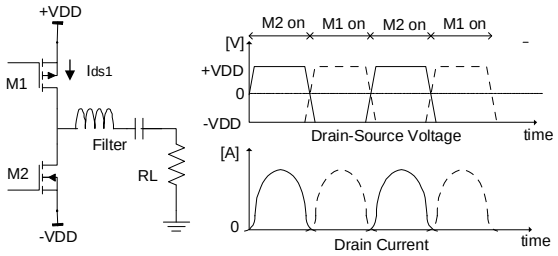
Switching-mode power amplifiers have the potential for high efficiency, with drain efficiency theoretically approaching 100%[1]. However, available transistors are not ideal switches because of parasitic reactances and finite on-resistance. Class-D amplifiers are popular switching mode amplifiers for audio frequencies. However they exhibit poor efficiency at higher frequencies because parasitic reactances generate substantial loss [2]. If transistor switches have output shunt capacitance C (and not too large series inductance, then energy ½ CV^2 is dissipated each cycle, where V is the voltage across the transistor at switch closure.

The Class-E approach can solve some of these problems [3]. When the transistors turn on and the switches close, the voltage across the devices is always zero, so output capacitance discharge loss is avoided (Zero-Voltage-Switching, ZVS). This approach works well in the MHz frequency range but is less effective in the GHz range. Variable duty-cycle, non-linear capacitances, and other parasitic components degrade the Class-E operation. Multiharmonic load termination [4], Class-F [5] and Inverse Class-F [6-7] are other, less well-developed, techniques to achieve ZVS (or Zero-Current-Switching, ZCS, a related condition which minimize series inductances losses).

Here we describe another approach that can achieve ZVS, the Current-Mode Class D (CMCD) Amplifier. This is related to the more frequently used Voltage-Mode Class D amplifier by an interchange between voltage and current waveforms. In this work the CMCD is demonstrated with GaAs FETs >75% power-added efficiency at 900MHz.

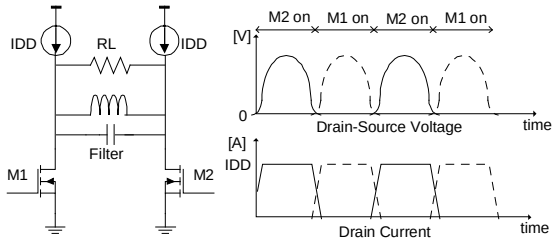
II. Concept Of Current Mode Class-D

Fig. 1(a) shows the basic schematic of a Voltage Mode Class-D (VMCD) amplifier (sometimes referred to only as "Class-D"). Two transistors are driven 180 degrees out of phase. A series filter is employed, with a resonant frequency set to the center frequency of the signal. Fig. 1(b) shows ideal voltage and current waveforms for this amplifier. The voltage across the transistors is a square wave and the transistor current becomes a half-wave rectified sinewave. In this case, the transistor's output capacitance C_{ds} must be charged or discharged to +VDD or –VDD through the transistor. Independent of channel resistance, this leads to a loss of ½$C_{ds}VDD^2$ energy for each switching cycle, per transistor. The C_{ds} capacitance discharge loss is more dominant than the Ron loss at high frequencies. As long as there is voltage across the transistor at the instant of switching, the capacitance



(a) (b)

Fig. 1 Voltage-Mode Class-D



(a) (b)

Fig. 2 Current-Mode Class-D

discharge loss cannot be avoided.

Fig. 2(a) shows the CMCD topology. In this case we use current sources instead of voltage sources, and the two switching transistors control the current instead of the voltage. There is a parallel-connected filter, with resonant frequency set to the carrier frequency. Fig.2 (b) shows the ideal current and voltage waveforms of the transistors. There is no voltage across the transistors at each switching time. Even if the transistors have some output capacitance, the output capacitance can become part of the output parallel filter; voltage waveforms are still as shown in Fig 2(b). This ZVS feature is a key advantage of the CMCD architecture.

As mentioned above, another important switching condition, Zero Current Switching (ZCS) avoids inductance losses by making the current zero at the instant of switching. VMCD and Class-F achieve this condition. However ZCS is less important than ZVS. Fig. 3(a) and (b) show examples of switches with parasitic inductance and capacitance in different topologies. In case (a) the capacitance voltage and the switch voltage are identical. So if there is voltage when the switches turn on, ½ CV^2 energy is lost, and ZVS is needed to avoid this loss. However, current can continue to flow to the capacitor when switches turn off and the inductance loss is eliminated. On the contrary, the capacitance loss is eliminated and inductance loss ½ LI^2 is unavoidable without ZCS in case (b). For most transistors are modeled more accurately in case (a) than case (b).

Another good feature of the CMCD amplifier is easy implementation at high frequency. The VMCD amplifier typically requires complementary devices or a center tapped transformer to function properly. The CMCD amplifier only requires a simple balun structure.

III. PA Design and Simulation

The CMCD amplifier was implemented at 900 MHz with commercially available GaAs MESFETs (Infineon CLY5). Harmonic balance simulations were performed with HP ADS. Statz MESFET model parameters of the chip transistor and the SOT223 package model were used. A simulation circuit is shown in Fig. 4 (minor package parasitic components are omitted in this figure). Due to practical board layout constraints, 25ohm transmission lines T1 and T2 are inserted between components. We optimized the lengths of T1 and T2, and the values of C_{ext} and C_{fil} to achieve ZVS at node A by simulation. Fig.4 shows simulated voltage and current waveforms. Solid lines indicate chip drain-source voltage and current, and dotted lines are voltage and current including package parasitic components (mainly L_{ind} and C_{ds}). Because of

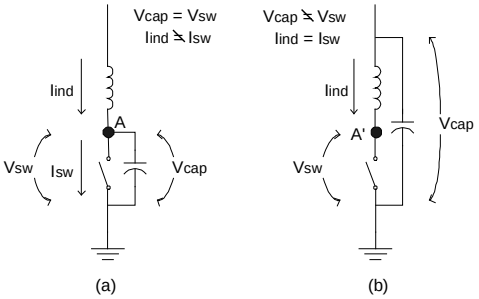


Fig 3. Switch models

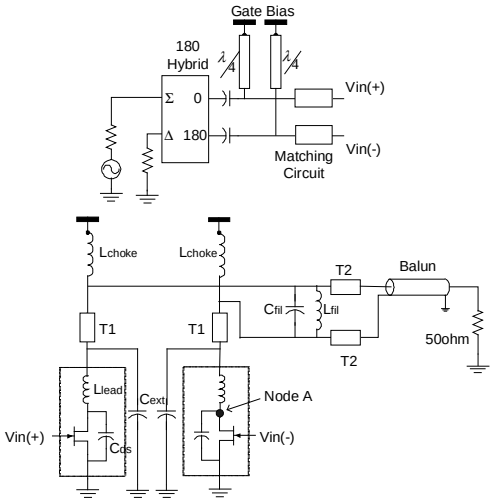
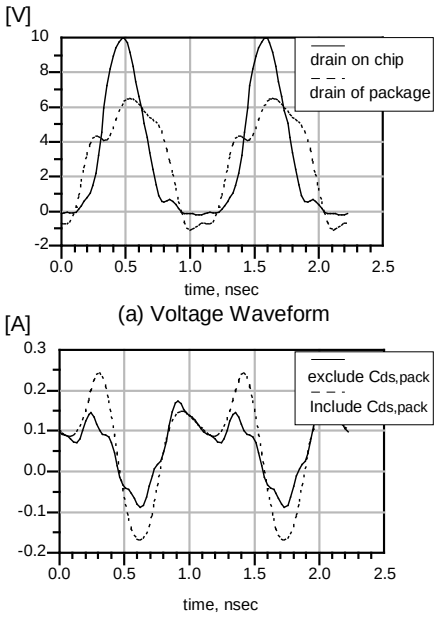


Fig 4. The CMCD Circuit



(a) Voltage Waveform

(b) Current Waveform

Fig 5. Simulated Waveforms

C_{ds}, the drain current is not an ideal square wave but becomes negative when the transistor is off. If we extract all capacitances (including device capacitances), the current waveform should be more rectangular. In this simulation, we achieved 84% PAE at 25.4dBm (0.35W) with VDD = 3V.

IV. Experimental Results

A picture of the CMCD power amplifier is shown in Fig. 6. A Mini-Circuits 180-degree hybrid is used to generate the balanced signal for the input and the input impedance matching circuits are tuned for maximum gain. C_{ext} and C_{fil} in Fig.4 are optimized for higher efficiency.

Fig. 7 shows the efficiency and RF output power when the gate bias voltage is –1.7V and VDD is 3V. The input power doesn't include the 180-hybrid loss but the output power includes output balun loss. The drain efficiency reaches 80% when the input power is above 11dBm. The P.A.E. reaches a peak value of 76.3% under these conditions. The corresponding power gain is approximately 12 dB. The gain decreases with increasing input power, since the output power is nearly constant (and determined only by the power supply voltage).

Fig. 8 shows the output power and efficiency when VDD is 5V. Drain efficiency of 75.6% and P.A.E of 72.5% was achieved with the input power set to 14.7dBm and output at 28.6dBm (0.73W).

In the regime of low input power (less than 6dBm in low power, less than 10dBm for high power), the CMCD works as a Class-AB push pull amplifier (because the parallel filter is an open circuit at the operational frequency). Thus, the structure is an approximately linear amplifier in this regime.

Fig. 9 shows the frequency dependence of output power and P.A.E. The dotted line shows the CMCD optimized for 900MHz. The solid line shows the case where the input matching circuits were tuned with variable capacitors at every frequency. This eliminates some of the frequency dependence of the input matching circuits. In this case, the power output becomes almost flat and PAE is greatly improved. This indicates that much of the circuit's bandwidth is a result of input impedance matching. From the standpoint of harmonic tuning, 2nd harmonics should be presented with an open and 3rd harmonics should be shorted for the CMCD (the same as for inverse class-F). Balanced circuits are intrinsically open at even harmonics and output capacitances of the transistors and filter tend to be shorted at high frequency. These two are less dependent on the operational frequency and the output load impedance. We believe the

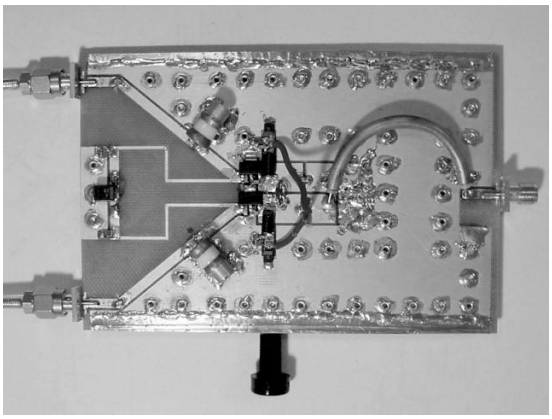


Fig. 6 The Picture of CMCD PA Circuit

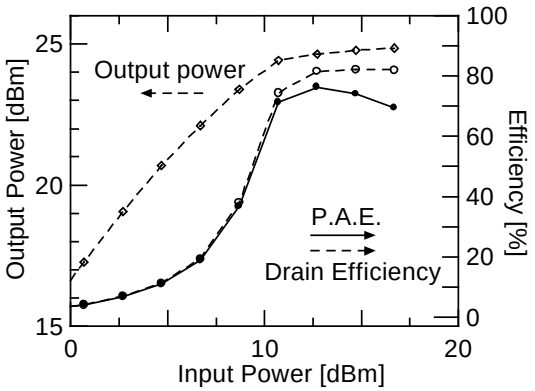


Fig. 7 Measured output power and Efficiency (VDD = 3V)

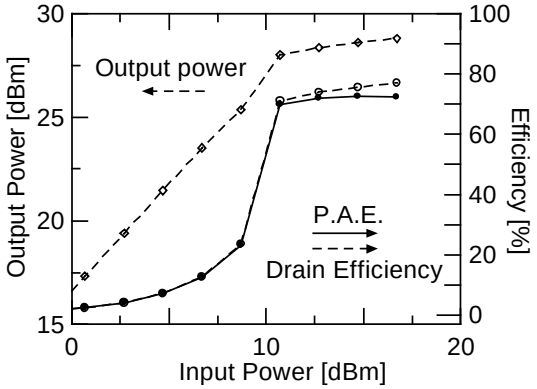


Fig. 8 Measured output power and Efficiency (VDD = 5V)

CMCD is capable of a large bandwidth when broadband impedance input matching is used.

V. System Application

The output of the CMCD amplifier has a nearly constant envelope, dictated by the power supply voltage. It is thus appropriate for use with modulated signals of constant envelope. Fig. 10 shows the output spectrum when a GSM modulated input signal was used (Pin=12.7dBm, VDD=3 and 5). No major distortion is observed in both cases. The drain efficiency and PAE values were equal to those measured for sinusoidal signals, as shown in Fig. 6 and 7. To apply the CMCD to QPSK or related waveforms with time-varying envelope, a modulated power supply voltage is required (such as in the Kahn technique).

VI. Conclusion

We demonstrated for the first time the possibility of current-mode class-D power amplifiers at RF frequencies. Experimental results confirm that high efficiency can be attained and show the possibility of high bandwidth.

ACKNOWLEDGEMENT

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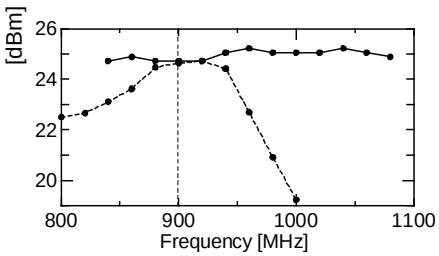
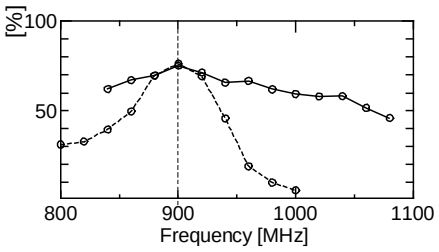


(a) Output Power



(b) PAE

Fig. 9 Output Power and P.A.E. vs. Frequency

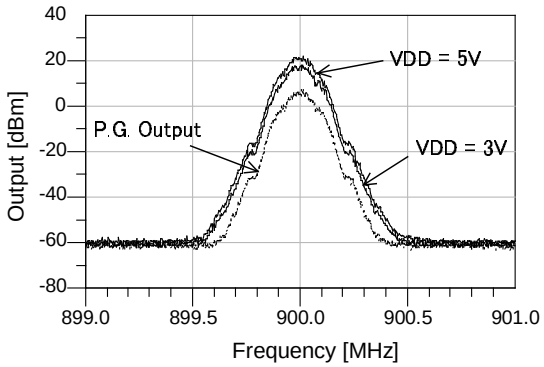


Fig. 10 Output Spectrum of GSM signal

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